Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (Currently Amended) An equalization circuit, comprising:

an input adapted to receive signals from a communications channel;

a plurality of equalizer circuits coupled to the input and operable to generate a plurality of intermediate signals;

a selector circuit, responsive to the plurality of equalizer circuits, that selects one of the intermediate signals; and

an output coupled to the selector circuit that receives the selected intermediate signal; and

a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for a selected period of time.

2. (Original) The equalization circuit of claim 1, wherein each of the plurality of equalizer circuits comprises one of a fixed equalizer and an adaptive equalizer.

3. (Original) The equalization circuit of claim 2, wherein each of the adaptive equalizers comprises one of a linear equalizer and a nonlinear equalizer.

4. (Original) The equalization circuit of claim 2, wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure.

5. (Original) The equalization circuit of claim 2, wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm.

6. (Original) The equalization circuit of claim 1, wherein the plurality of equalizer circuits provides a signal that reflects the relative quality of the intermediate signals from the plurality of equalizer circuits to the selector circuit to select the intermediate signal.

7. (Cancelled)

8. (Currently Amended) The equalization circuit of claim ~~7~~1, wherein the buffer circuits buffer the intermediate signals for approximately the duration of a time slot of the communication channel.

9. (Original) An equalization circuit, comprising:

an input adapted to receive signals from a communication channel;

an equalizer bank having at least two equalizers coupled in parallel and coupled to the input;

a decoder bank having at least two error correction decoder circuits coupled in parallel, each error correction decoder circuit coupled to a corresponding one of the at least two equalizers of the equalizer bank;

a selector circuit coupled to the decoder bank that selects an output signal of one of the at least two equalizer circuits based on processing of the decoder bank; and

an output coupled to the selector circuit that receives the selected output signal.

10. (Original) The equalization circuit of claim 9, wherein the decoder bank includes at least two forward error correction decoder circuits.

11. (Original) The equalization circuit of claim 9, wherein each of the at least two equalizers comprises one of a fixed equalizer and an adaptive equalizer.

12. (Original) The equalization circuit of claim 11, wherein each of the adaptive equalizers comprises one of a linear equalizer and a nonlinear equalizer.

13. (Original) The equalization circuit of claim 11, wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure.

14. (Original) The equalization circuit of claim 11, wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm.

15. (Previously Presented) The equalization circuit of claim 9, wherein the decoder bank provides a feedback signal to the at least two equalizers of the equalizer bank.

16. (Original) The equalization circuit of claim 15, wherein the feedback signal is also provided to the selector circuit to be used in selecting the output of one of the at least two equalizer circuits.

17. (Original) The equalization circuit of claim 9, wherein the decoder bank includes a buffer circuit with each of the at least two error correction decoder circuits.

18. (Original) An equalization circuit, comprising:

an input adapted to receive signals from a communication channel;

an equalizer bank having at least two equalizers coupled in parallel and coupled to the input;

a first decoder bank having at least two packet decoder circuits coupled in parallel, each packet decoder circuit responsive to a corresponding one of the at least two equalizers of the equalizer bank;

a selector circuit coupled to the decoder bank that selects an output signal of one of the at least two equalizer circuits based on processing of the decoder bank; and

an output coupled to the selector circuit that receives the selected output signal.

19. (Original) The equalization circuit of claim 18, and further comprising a second decoder bank having at least two error correction decoder circuits coupled in parallel, each error correction decoder circuit coupled to a corresponding one of the at least two equalizers of the equalizer bank and coupled to a corresponding one of the at least two packet decoder circuits.

20. (Original) The equalization circuit of claim 19, wherein the second decoder bank includes at least two forward error correction decoder circuits.

21. (Original) The equalization circuit of claim 18, wherein each of the at least two equalizers comprises one of a fixed equalizer and an adaptive equalizer.

22. (Original) The equalization circuit of claim 21, wherein each of the adaptive equalizers comprises one of a linear equalizer and a nonlinear equalizer.

23. (Original) The equalization circuit of claim 21, wherein each of the adaptive equalizers comprises one of a transversal structure and a lattice structure.

24. (Original) The equalization circuit of claim 21, wherein each of the adaptive equalizers uses one of a recursive least squares adaptation algorithm, a least mean-square adaptation algorithm, a zero forcing adaptation algorithm, a gradient recursive least squares adaptation algorithm, a fast recursive least squares adaptation algorithm and a square root recursive least squares adaptation algorithm.

25. (Previously Presented) The equalization circuit of claim 18, wherein the first decoder bank provides a feedback signal to the at least two equalizers of the equalizer bank.

26. (Original) The equalization circuit of claim 25, wherein the feedback signal is also provided to the selector circuit to be used in selecting the output of one of the at least two equalizer circuits.

27. (Original) The equalization circuit of claim 18, wherein the at least two packet decoder circuits comprise decoder circuits that process cyclic redundancy checks (CRCs) for Ethernet packets.

28. (Previously Presented) A method for equalizing a signal from a time division multiple access communication channel, the method comprising:

receiving a signal over the communication channel;

equalizing the signal in a plurality of equalizers;

selecting an output of one of the equalizers; and

buffering the output of the plurality of equalizers;

wherein buffering the output of the plurality of equalizers comprises buffering the output of the plurality of equalizers for the duration of a time slot of the communication channel.

29. (Original) The method of claim 28, wherein receiving a signal over the communication channel comprises receiving the signal over a wireless communication channel.

30. (Original) The method of claim 28, wherein receiving a signal over the communication channel comprises receiving the signal over a communication channel of a hybrid fiber-coax network.

31. (Original) The method of claim 28, wherein equalizing the signal comprises equalizing the signal in a bank of equalizers.

32. (Original) The method of claim 31, and further comprising loading selected coefficients for a plurality of equalizers prior to receiving a signal over the communication channel.

33. (Cancelled)

34. (Cancelled)

35. (Original) The method of claim 28, and further comprising generating a quality measure of the output of each of the plurality of equalizers.

36. (Original) The method of claim 28, wherein generating a quality measure comprises generating one of a mean-squared error and a peak error over a selected interval.

37. (Previously Presented) A method for equalizing a signal from a time division multiple access communication channel, the method comprising:

receiving a signal over the communication channel;

equalizing the signal in parallel in a bank of adaptive equalizers with parallel outputs;

buffering parallel outputs of the bank of adaptive equalizers;

further processing the parallel outputs of the bank of adaptive equalizers;

generating a quality measure of the output of each of the bank of adaptive equalizers; and

selecting an output of one of the equalizers based on the quality measure;

wherein buffering the parallel outputs comprises buffering the parallel outputs for the duration of a time slot of the communication channel.

38. (Original) The method of claim 37, wherein receiving a signal over the communication channel comprises receiving the signal over a wireless communication channel.

39. (Original) The method of claim 37, wherein receiving a signal over the communication channel comprises receiving the signal over a communication channel of a hybrid fiber-coax network.

40. (Original) The method of claim 37, wherein further processing the parallel outputs comprises forward error correcting the parallel outputs.

41. (Original) The method of claim 37, wherein further processing the parallel outputs comprises detecting errors at the packet level.

42. (Cancelled)

43. (Currently Amended) An equalization circuit, comprising:

an input adapted to receive signals from a communications channel;

at least one equalizer circuit coupled to the input and operable to generate at least one intermediate signal;

a selector circuit, responsive to the at least one equalizer circuit, that selects between the intermediate signal and the signal received at the input; ~~and~~

an output coupled to the selector circuit that receives the selected intermediate signal or the signal received at the input; and

a plurality of buffer circuits, each buffer circuit coupled between each of the at least one equalizer circuits and the selector circuit to buffer the intermediate signals for a selected period of time.

44. (Original) The equalization circuit of claim 43, wherein the at least one equalizer comprises an adaptive equalizer.

45. (Original) A method for equalizing a signal from a time division multiple access communication channel, the method comprising:

loading coefficients for a selected time slot of the communication channel into a plurality of parallel equalizers;

receiving a signal from the communication channel;

equalizing the signal in the plurality of equalizers to produce a plurality of equalized signals;

further processing the equalized signals with at least one plurality of parallel decoder circuits; and

selecting one of the processed, equalized signals based on one of the equalizing and the further processing.

46. (Original) The method of claim 45, wherein equalizing the signal comprises equalizing the signal with a plurality of adaptive equalizers.

47. (Original) The method of claim 45, wherein further processing the equalized signals comprises forward error correcting the equalized signals.

48. (Original) The method of claim 45, wherein further processing the equalized signals includes checking for errors at the packet level.

49. (Currently Amended) A telecommunications system, comprising:

at least one base station adapted to provide a connection to a core network;

the base station including a circuit that receives signals from the core network and provides the signals to a plurality of remote users over at least one communication channel;

the base station further including a receiver that receives time division multiple access signals from a plurality of remote users over at least one communication channel; and

wherein the base station includes an equalization circuit, the equalization circuit including:

a plurality of equalizer circuits coupled to receive signals from the at least one communication channel and operable to generate a plurality of intermediate signals;

a selector circuit, responsive to the plurality of equalizer circuits, that selects one of the intermediate signals; ~~and~~

an output coupled to the selector circuit that receives the selected intermediate signal and provides the signal to the connection to the core network; and

a plurality of buffer circuits, each buffer circuit coupled between one of the plurality of equalizer circuits and the selector circuit to buffer the intermediate signals for a selected period of time.

50. (Original) The system of claim 49, wherein the base station comprises a wireless base station.

51. (Original) The system of claim 49, wherein the base station comprises a head end of a hybrid fiber-coax network.